

# Resistive switching memories: hardware components for AI

## Memristors

*Resistive switching random access memory (RRAM)* usually refers to resistance-variable, two-terminal metal/insulator/metal nanostructures. These devices are also called *memristors* (blending the words "memory" + "resistor"), since the basis for information storage is the device resistance. Electrical control of the resistance is usually achieved by applying various electrical signals to the device, exceeding the threshold value for resistive switching, as illustrated in Fig. 1. For *bipolar* devices, typical  $I(V)$  characteristics are shown upon applying triangular signals in Fig. 1(a). Starting at a higher resistance, so-called OFF state, the resistance is usually perceived as a constant value at first, for low voltages. Once the switching threshold is reached at positive direction, resistive switching occurs, current increases, and the device arrives at a different, lower resistance ON state, usually referred to as the *set* process. Similarly, *reset* process can be achieved by applying voltage of opposite polarity for bipolar devices (as seen in Fig. 1(a)). A usual circuit for the measurement of  $I(V)$  characteristics is shown in Fig. 1(b). An  $R_s$  serial resistance is connected to the  $R_m$  memristor. The role of the serial resistance is to limit the current, terminating the set process when the ON-state resistance approaches  $R_m \approx R_s$ .

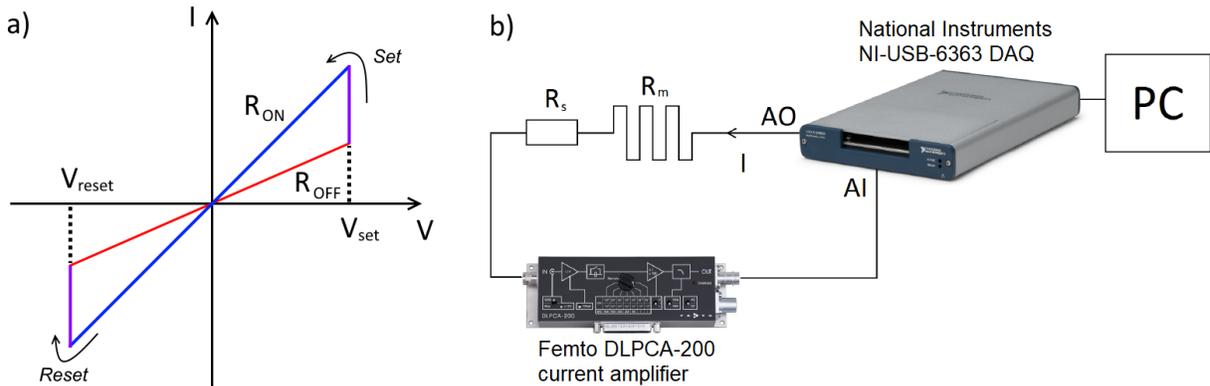


Figure 1: (a) Typical bipolar  $I(V)$  characteristics of memristors, and (b) circuit diagram for the measurement of  $I(V)$  curves. A resistive switching memory ( $R_m$ ) is connected with a serial resistance ( $R_s$ ), which limits the current during the set process.

A vast number of nanomaterials exhibit resistive switching behaviour, and many physical mechanisms can contribute to the resistive switching phenomenon in each of them [1, 2, 3]. A typical classification of resistive switching cells is based on the governing physical processes (as illustrated in Fig. 2.):

- For certain devices, the active region acts as a solid electrolyte sandwiched between active and inert electrodes. Metal ions from the active electrode start to migrate inside the active region, which is usually a compound of the active metal. As a result, a nanoscale metallic filament is formed between the electrodes in an *electro-chemical metallization (ECM)* process.

- In metal oxide-based cells, oxygen vacancies are involved in resistive switching, usually referred to as *valence change mechanism (VCM)*. A filament can be composed of these vacancies, resulting in an oxygen-deficient metallic region connecting the electrodes. Furthermore, oxygen vacancies can act as mobile/immobile charge traps (depending on the device composition), and these charge trapping-detrapping effects can also play substantial role in resistive switching in VCM cells.
- The operation principle of *phase-change memories (PCM)* is rather different from the latter two groups [4]. In PCM devices, crystallization/amorphization of the active region leads to resistive switching effects. Amorphization usually involves melting of the inner, phase-change material (via Joule heating), and due to fast cooling, the material quenches in a disordered, amorphous state. Temperature also plays role in the crystallization process. In this case, besides heating of the cell (far below the melting point), crystallization usually occurs in an electric field-induced manner with thermal activation.

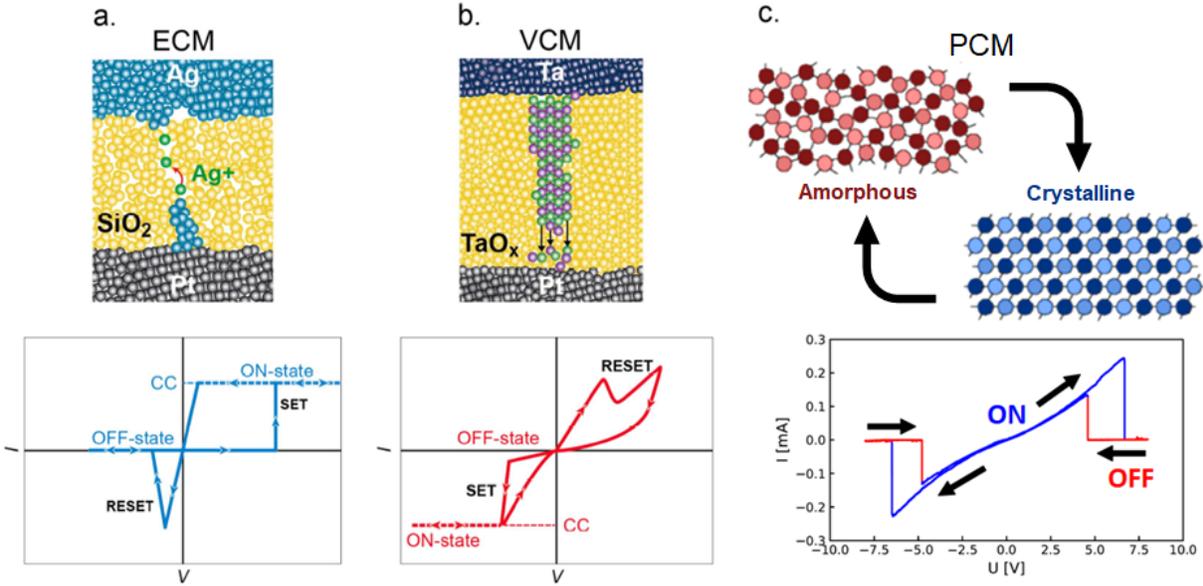


Figure 2: Illustration of different processes in resistive switching memories. [5, 6, 7].

## ECM and VCM cells as analogue memories

One important property for analogue memory applications is the multilevel programmability of memristors. Various states with different resistances can be achieved by tuning the amplitude and frequency of the driving voltage signals. The latter property of resistive switching devices is usually referred to as *time-voltage dilemma*. STM point-contact mode is an efficient mode for studying resistive switching materials. These point-contact samples are initialized in an STM setup, by touching the PtIr tip to the surface of a thin layer sample. For example, a PtIr/Ag<sub>2</sub>S/Ag STM point-contact operates as an ECM-type cell, in which the filament is formed of silver. Varying the driving voltage amplitude and signal frequency affects the resistance ratio of a junction as shown in Fig. 3 [8]. When the driving signal frequency is increased, while the amplitude is kept constant, the hysteresis loop closes, and the  $R_{\text{OFF}}/R_{\text{ON}}$  ratio decreases (see Fig. 3(b)). If the driving triangular

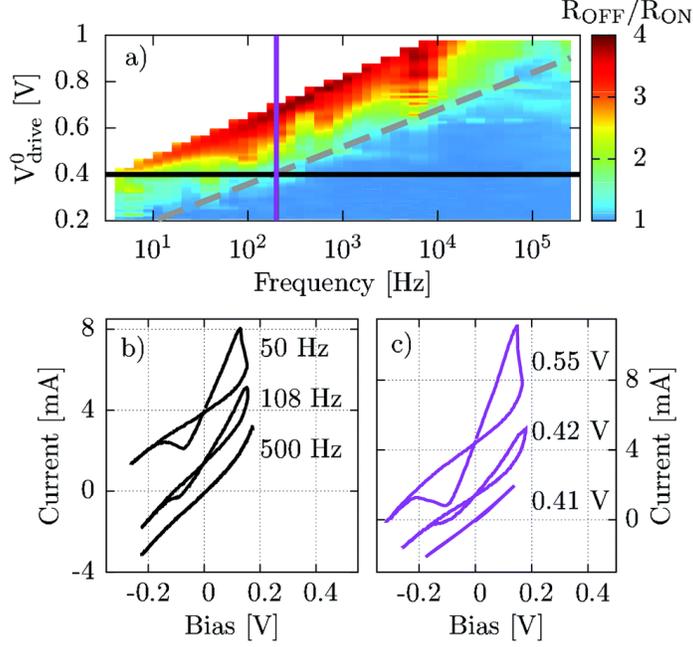


Figure 3: *Examples for the time-voltage dilemma in PtIr/Ag<sub>2</sub>S/Ag STM point-contact junctions [8].*

voltage amplitude is increased (while the frequency is kept constant), the hysteresis curve opens up, which means greater  $R_{\text{OFF}}/R_{\text{ON}}$  resistance ratios, as shown in Fig. 3(c).

However, PtIr/Ta<sub>2</sub>O<sub>5</sub>/Ta STM point-contact junctions operate via VCM, leading to differently shaped  $I(V)$  characteristics than Ag<sub>2</sub>S. Yet, the same time-voltage dilemma is observable in Ta<sub>2</sub>O<sub>5</sub>-based devices as well (see Fig 4.). Multiple states are achievable with these memristors, furthermore, Ta<sub>2</sub>O<sub>5</sub> switching medium offers other remarkable properties for analogue memory applications as well:  $\sim 100$  ps switching times [9], endurance of  $10^{12}$  switching cycles [10], and  $\sim$ pJ switching energies [11]. Fuelled by these beneficial properties, development of Pt/Ta<sub>2</sub>O<sub>5</sub>/Ta crosspoint devices recently began in our group.

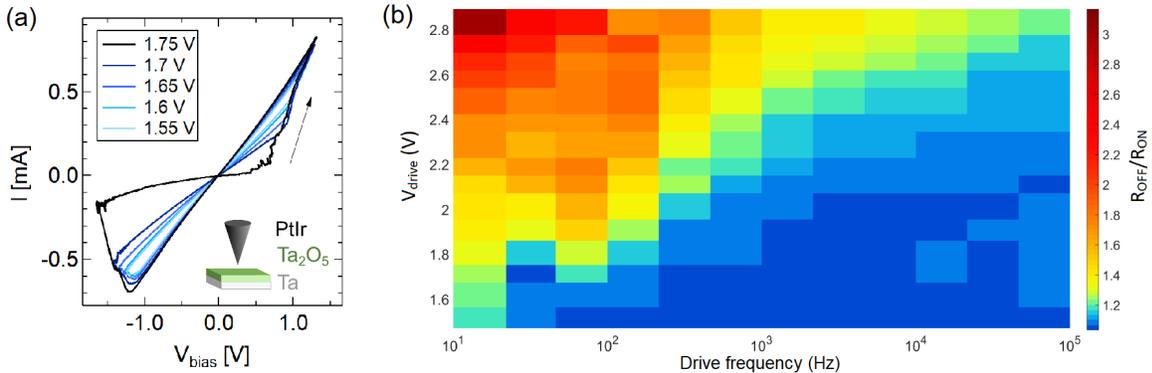


Figure 4: *Examples for the time-voltage dilemma in PtIr/Ta<sub>2</sub>O<sub>5</sub>/Ta STM point-contact junctions [12].*

## Hardware implementation of neural networks

Memristors are an emerging platform for novel information technologies, since they are applicable as hardware-based analog memories. Furthermore, in-memory computing is achievable with a network of resistive switching devices, with the *crossbar* architecture illustrated in Fig. 5. In such a crossbar device, resistive switching elements are located at each crosspoint, and matrices can be encoded as  $G_{ij}$  conductance values. When different  $V_i$  voltage values – representing a vector – are applied to each row of the crossbar, the column-wise  $I_j$  current values are the results of  $I_j = \sum V_i G_{ij}$  vector-matrix multiplication, computed in a single step – via Kirchhoff’s law and Ohm’s law. These hardware-based neural networks offer orders of magnitude acceleration and significantly less energy consumption compared to state-of-the-art GPU-based networks [13].

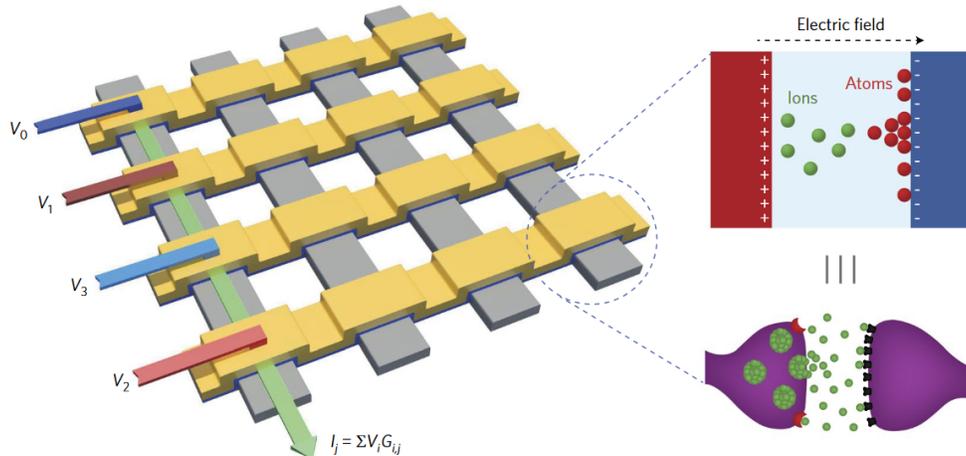


Figure 5: *Illustration of a crossbar memristor architecture for the hardware implementation of neural networks. Memristors located at each crosspoint can mimic the behaviour of biological synapses, facilitating bio-inspired computing schemes [3].*

## Measurement tasks

The goal is the experimental study of Pt/Ta<sub>2</sub>O<sub>5</sub>/Ta crosspoint RRAM samples. SEM image of the crosspoint devices is shown in Fig. 6.(a). These devices have bipolar  $I(V)$  characteristics with slightly different threshold voltages for the *set* and *reset* processes (see Fig. 6.(b)).

- Find the correct voltage amplitudes in order to achieve  $R_{\text{OFF}}/R_{\text{ON}} \approx 10$ .
- Increase the driving signal frequency (while keeping the amplitudes constant), and close the hysteresis loop. After closing the loop, return to the starting parameters in the same manner.
- Try tuning the ON state by decreasing the positive (set) voltage amplitude, keeping the frequency and the negative amplitude constant. Return to the starting parameters in the same manner.

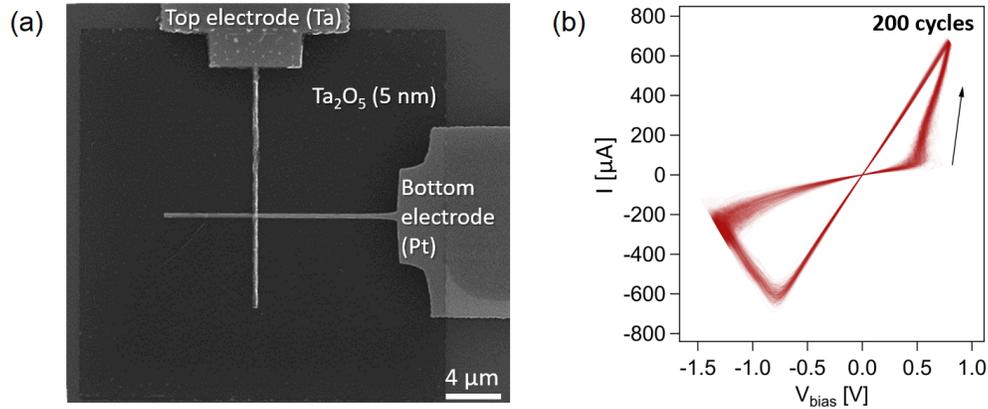


Figure 6: (a) SEM image of the vertical Pt/Ta<sub>2</sub>O<sub>5</sub>/Ta crosspoint RRAM samples, and (b) typical  $I(V)$  curves of the devices.

## Measurement control

The circuit used for the measurements is shown in Fig. 1.(b). Fig. 7. shows the user interface of the program used for recording  $I(V)$  characteristics. The value of serial resistance and gain setting of the *Femto* amplifier must be given to the program manually. A constant DC voltage can be applied to the sample with the "Bias Voltage" switch. The parameters of the triangular waveform can be set in the "IV parameters" box. The waveform is built up of 12000 points (this value is hard-coded in the program), and the sample rate can be calculated accordingly for a desired driving signal frequency.

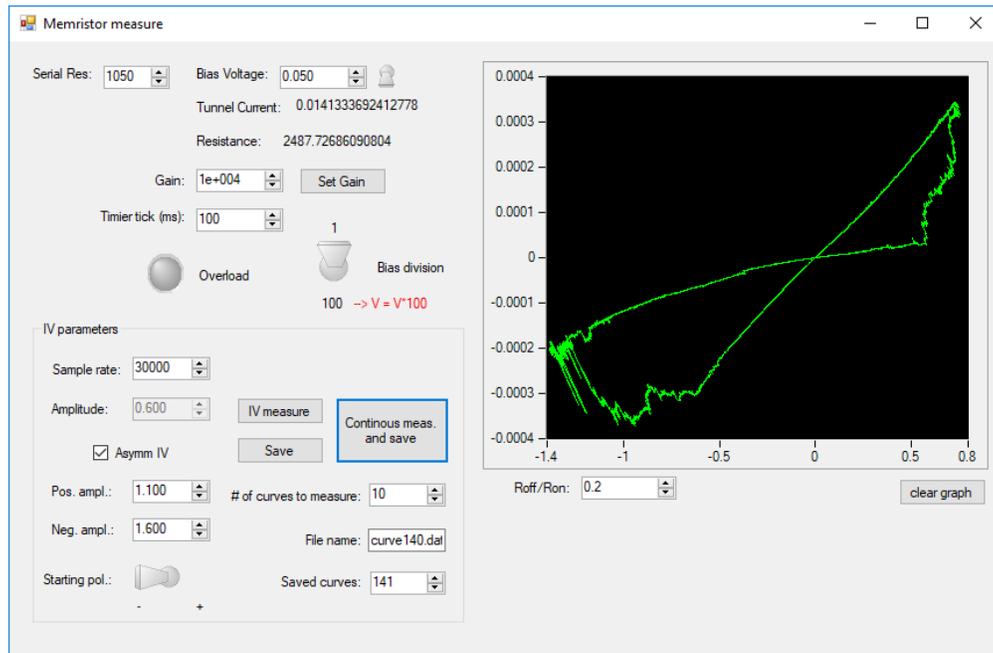


Figure 7: User interface of the program used for recording  $I(V)$  characteristics.

## References

- [1] J. J. Yang, D. B. Strukov, and D. R. Stewart. *Memristive devices for computing*. Nature Nanotechnology, **8**, 13 (2013).
- [2] Q. Xia and J. J. Yang. *Memristive crossbar arrays for brain-inspired computing*. Nature Materials, **18**, 309 (2019).
- [3] M. A. Zidan, J. P. Strachan, and W. D. Lu. *The future of electronics based on memristive systems*. Nat. Electron., **1**, 22 (2018).
- [4] M. Le Gallo and A. Sebastian. *An overview of phase-change memory device physics*. Journal of Physics D: Applied Physics, **53**, 213002 (2020).
- [5] I. Valov. *Interfacial interactions and their impact on redox-based resistive switching memories (ReRAMs)*. Semiconductor Science and Technology, **32**, 093006 (2017).
- [6] J. G. Fehérvári. *Experimental study of time-scales in nanoscale phase change memories*. TDK thesis, BME (2020).
- [7] L. Posa, M. Abbassi, P. Makk, B. Santa, C. Nef, M. Csontos, M. Calame, and A. Halbritter. *Multiple physical timescales and dead time rule in few-nm sized graphene-SiO<sub>x</sub>-graphene memristors*. Nano Letters, **17**, 6783 (2017).
- [8] A. Gubicza, M. Csontos, A. Halbritter, and Gy. Mihály. *Non-exponential resistive switching in Ag<sub>2</sub>S memristors: a key to nanometer-scale non-volatile memory devices*. Nanoscale, **7**, 4394 (2015).
- [9] A. C. Torrezan, J. W. Strachan, G. Medeiros-Ribeiro, and R. S. Williams. *Sub-nanosecond switching of a tantalum oxide memristor*. Nanotechnology, **22**, 485203 (2011).
- [10] M.-J. Lee, C. B. Lee, D. Lee, S. Lee, M. Chang, J. Hur, Y.-B. Kim, C.-J. Kim, D. Seo, S. Seo, U.-I. Chung, I.-K. Yoo, and K. Kim. *A Fast, High-Endurance and Scalable Non-Volatile Memory Device Made from Asymmetric Ta<sub>2</sub>O<sub>5-x</sub>/TaO<sub>2-x</sub> Bilayer Structures*. Nature materials, **10**, 625 (2011).
- [11] J. J. Yang, M.-X. Zhang, J. P. Strachan, F. Miao, M. D. Pickett, R. D. Kelley, G. Medeiros-Ribeiro, and R. S. Williams. *High switching endurance in TaOx memristive devices*. Applied Physics Letters, **97**, 232102 (2010).
- [12] C. Sinkó. *Átmenetifém-oxid memrisztorok kísérleti vizsgálata pont-kontaktus technikával*. BSc thesis, BME (2018).
- [13] S. Ambrogio, P. Narayanan, H. Tsai, R. Shelby, I. Boybat, C. Nolfo, S. Sidler, M. Giordano, M. Bordini, N. Farinha, B. Killeen, C. Cheng, Y. Jaoudi, and G. Burr. *Equivalent-accuracy accelerated neural-network training using analogue memory*. Nature, **558** (2018).